EXHIBIT A

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Renee M. Franks
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March 23, 2006
Date

APPLICATION NO.	10/676,739
FILING DATE	09/30/2003
FIRST NAMED INVENTOR	William B. Boyle, et al.
ART UNIT	2186
CONFIRMATION NO.	7957
EXAMINER	Paul W. Schlie
ATTORNEY DOCKET NO.	K35A1281

TITLE: REDUCING MICRO-CONTROLLER ACCESS TIME TO DATA STORED IN A REMOTE MEMORY IN A DISK DRIVE CONTROL SYSTEM

ATTACHED WITH THIS SUBMISSION:

1. Transmittal Form (1 page)
2. Response Under 37 C.F.R. § 1.111 to Office Action dated October 25, 2005 (10 pages)

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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission

Application Number	10/676,739
Filing Date	09/30/2003
First Named Inventor	William B. Boyle, et al.
Art Unit	2186
Examiner Name	Paul W. Schlie
Attorney Docket Number	K35A1281

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☑ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Western Digital		
Signature			
Printed name	Jason T. Evans, Esq.		
Date	March 23, 2006	Reg. No.	57,862

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I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

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Typed or printed name	Renee M. Franks	Date	March 23, 2006

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Appln. of:	William B. Boyle, et al.	Art Unit:	2186
Serial No.:	10/676,739	Examiner:	Paul W. Schlie
Filing Date:	09/30/2003	Confirmation No.:	7957
For: REDUCING MICRO-CONTROLLER ACCESS TIME TO DATA STORED IN A REMOTE MEMORY IN A DISK DRIVE CONTROL SYSTEM		Docket No.:	K35A1281

REPLY UNDER 37 C.F.R. § 1.111
TO OFFICE ACTION DATED OCTOBER 25, 2005

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Office Action mailed on October 25, 2005 for the above-identified patent application, please consider the following amendments and remarks. Please also note that the shortened statutory period was reset to run from January 3, 2006, based on a Decision Granting Applicant's Petition to Reset Period for Reply mailed on February 1, 2006.

Amendments to the **Claims** are reflected in the listing of claims that begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

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AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) In a disk drive control system comprising a micro-controller, a micro-controller cache system having a plurality of line-cache segments grouped into at least one line-cache segment-group, and a buffer manager communicating with the micro-controller cache system and a remote memory, a method for reducing the micro-controller access time to information stored in the remote memory via the buffer manager, the method comprising:

receiving in the micro-controller cache system a current data-request from the micro-controller; and

if the current requested data resides in a first line-cache segment of a first segment-group:

providing the current requested data to the micro-controller ~~if the current requested data resides in a first line-cache segment of a first segment-group~~; and

automatically filling a second line-cache segment of the first segment-group with data retrieved from the remote memory wherein the retrieved data is sequential in the remote memory to the provided current requested data if the second line-cache segment hosted a most-recently requested data prior to the current requested data.

2. (Canceled)

3. (Currently Amended) The method of claim 21, wherein the automatically filling further comprises:

filling the second line-cache segment if the current requested data is sequential to the most-recently requested data.

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4. (Original) The method of claim 1, wherein the retrieved data comprises a burst of data in the range of 32 to 64 bytes.

5. (Original) The method of claim 1, wherein the plurality of line-cache segments are grouped into a plurality of line-cache segment-groups.

6. (Currently Amended) The method of claim 5, further comprising:

if the current requested data does not reside in the plurality of line-cache segment-groups:

selecting a line-cache segment-group ~~if the current requested data does not reside in the plurality of line-cache segment-groups~~;

filling a first line-cache segment of the selected line-cache segment-group with a first set of data from the remote memory location wherein the first set of data comprises the current requested data;

providing the current requested data to the micro-controller from the filled first line-cache segment; and

filling a second line-cache segment of the selected line-cache segment-group with a second set of data from the remote memory location wherein the second set of data is sequential in the remote memory to the first set of data.

7. (Original) The method of claim 6, wherein the selected line-cache segment-group is a least recently used line-cache segment-group.

8. (Original) The method of claim 6, wherein the first set of data comprises a first burst of data in the range of 32 to 64 bytes.

9. (Original) The method of claim 6, wherein the second set of data comprises a second burst of data in the range of 32 to 64 bytes.

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10. (Original) The method of claim 1, wherein the line-cache segment-group comprises two line-cache segments.

11. (Original) The method of claim 1, wherein the remote memory comprises a dynamic random access memory (DRAM).

12. (Original) The method of claim 1, wherein the buffer manager is in communication with a plurality of control system clients and provides client-requested data to the clients from the remote memory.

13. (Original) The method of claim 12, wherein the plurality of control system clients comprises at least one of a disk subsystem, an error correction code subsystem, and a host interface subsystem.

14. (Currently Amended) A disk drive control system comprising:

a micro-controller,

a micro-controller cache system having a plurality of line-cache segments grouped into at least one line-cache segment-group, and

a buffer manager communicating with the micro-controller cache system and a remote memory, ~~the disk-drive control system comprising:~~

wherein the micro-controller cache system is adapted to: a) receive a current data-request from the micro-controller, and, if the current requested data resides in a first line-cache segment of a first segment-group, b) provide the current requested data to the micro-controller ~~if the current requested data resides in a first line-cache segment of a first segment-group~~, and c) automatically fill a second line-cache segment of the first segment-group with data retrieved from the remote memory wherein the retrieved data is sequential in the remote memory to the provided current requested data if the second line-cache segment hosted a most-recently requested data prior to the current requested data.

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15. (Canceled)

16. (Currently Amended) The disk drive control system of claim ~~15~~14, wherein the micro-controller cache system automatically fills the second line-cache segment if the current requested data is sequential to the most-recently requested data.

17. (Original) The disk drive control system of claim 14, wherein the plurality of line-cache segments are grouped into a plurality of line-cache segment-groups.

18. (Currently Amended) The disk drive control system of claim 17, wherein the micro-controller cache system is further adapted to, if the current requested data does not reside in the plurality of line-cache segment-groups, a) select a line-cache segment-group ~~if the current requested data does not reside in the plurality of line-cache segment-groups~~; b) fill a first line-cache segment of the selected line-cache segment-group with a first set of data from the remote memory location wherein the first set of data comprises the current requested data; c) provide the current requested data to the micro-controller from the filled first line-cache segment; and d) fill a second line-cache segment of the selected line-cache segment-group with a second set of data from the remote memory location wherein the second set of data is sequential in the remote memory to the first set of data.

19. (Original) The disk drive control system of claim 18, wherein the selected line-cache segment-group is a least recently used line-cache segment-group.

20. (Canceled)

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REMARKS

The Applicants thank the Examiner for his careful and thoughtful examination of the present application. By way of summary, Claims 1-20 were pending in this application. In the present amendment, the Applicants have canceled Claims 2, 15 and 20 without prejudice or disclaimer and amended Claims 1, 3, 6, 14, 16 and 18. Accordingly, Claims 1, 3-14 and 16-19 remain pending for consideration.

AMENDMENTS TO THE CLAIMS

Claim 1 has been amended to clarify the claim language, and to incorporate limitations from previously pending Claim 2. Claim 3 has been amended to depend properly from Claim 1. Claim 6 has been amended to clarify the claim language. Claim 14 has been amended to clarify the claim language, and to incorporate limitations from previously pending Claim 15. Claim 16 has been amended to depend properly from Claim 14. Claim 18 has been amended to clarify the claim language. The amendments to these claims have not been made for the purposes of patentability, and it is believed that the claims would satisfy the statutory requirements for patentability without the entry of such amendments

REJECTION UNDER 35 USC § 102(b)

The Office action rejected Claims 1-2, 4-15 and 17-19 under 35 U.S.C. § 102(b) as being anticipated by U.S. patent no. 6,360,299, issued to Arimilli *et al.* (the Arimilli patent). The Applicants respectfully traverse this rejection because the Arimilli patent fails to identically teach every element of the claims. See M.P.E.P. § 2131 (stating that in order to anticipate a claim, a prior art reference must identically teach every element of the claim).

In particular, amended Claim 1 recites a method for reducing micro-controller access time, comprising: "if the current requested data resides in a first line-cache segment of a first segment-group: providing the current requested data to the micro-controller; and automatically filling a second line-cache segment of the first segment-

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group with data retrieved from the remote memory wherein the retrieved data is sequential in the remote memory to the provided current requested data if the second line-cache segment hosted a most-recently requested data prior to the current requested data." These limitations of Claim 1 are not taught or suggested by Arimilli.

The Examiner asserts that Arimilli teaches to "automatically fill a subsequent second segment . . . which was most recently previously accessed relative to the most current request with corresponding sequentially accessed data (column 10 lines 27-28)." Office action, page 2. The Applicants respectfully disagree.

The Applicants submit that column 10, lines 27-31 recites: "[a]n additional bit 229 may optionally be utilized to indicate as between the two slots, which is the most recently used, for those cases wherein a prefetch request misses the L2 cache and both slots already have prefetched lines with different stream IDs." However, this passage does not teach the step of "automatically filling a second line-cache segment . . . if the second line-cache segment hosted a most-recently requested data," as recited by the amended claim.

Instead, Arimilli's method of selecting a next "victim" line for filling uses "a standard victim selection algorithm, such as a least-recently, or less-recently, used (LRU) algorithm, which is applied to all sets including the prefetched line." Col. 9, ll. 55-58. Thus, according to Arimilli's method, the line that has been least-recently used is used to receive new data. For example, Arimilli describes that "[w]hen a prefetch request misses the L2 cache and neither slot is allocated, a victim is selected using the standard LRU algorithm" (Col. 10, ll. 4-6), and "[t]he prefetch slots are not exclusively used for speculative requests; they may be used for non-prefetch requests if the standard LRU algorithm were to select[] that set for victimization" (Col. 10, ll. 11-14). Arimilli does not disclose any other algorithm for selecting the next line for victimization. Therefore, Arimilli does not disclose "automatically filling a second line-cache segment . . . if the second line-cache segment hosted a most-recently requested data." Instead, the additional bit 229 called out by the Examiner would likely be used to protect a slot, by preventing the most recently used slot from being victimized. Indeed, there is no

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disclosure or suggestion anywhere in Arimilli of automatically filling a line-cache segment if the most recently used bit 229 is set for that line-cache segment.

For at least these reasons, Applicants respectfully submit that the rejection of amended Claim 1 over Arimilli is improper, and the Applicants respectfully request allowance of Claim 1.

Claims 4-13, which depend from Claim 1, are believed to be patentable for at least the same reasons articulated above with respect to Claim 1, and because of the additional features recited therein.

Amended Claim 14 similarly recites a disk drive control system comprising a micro-controller cache system adapted to: "if the current requested data resides in a first line-cache segment of a first segment-group . . . automatically fill a second line-cache segment of the first segment-group with data retrieved from the remote memory wherein the retrieved data is sequential in the remote memory to the provided current requested data if the second line-cache segment hosted a most-recently requested data prior to the current requested data." These limitations of Claim 14 are not taught or suggested by Arimilli.

As discussed above, Arimilli does not teach a micro-controller cache system adapted to "automatically fill a second line-cache segment . . . if the second line-cache segment hosted a most-recently requested data," as recited by the claim. Therefore, for reasons similar to those discussed above, Applicants respectfully submit that the rejection of amended Claim 14 over Arimilli is improper, and the Applicants respectfully request allowance of Claim 14.

Claims 17-19, which depend from Claim 14, are believed to be patentable for at least the same reasons articulated above with respect to Claim 14, and because of the additional features recited therein.

REJECTION UNDER 35 USC § 103(a)

The Office action further rejected Claims 3 and 16 under 35 U.S.C. § 103(a) as being unpatentable over the Arimilli patent in view of U.S. patent no. 5,345,560, issued to Miura *et al.* (the Miura patent). The Applicants respectfully traverse this rejection

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because the Arimilli patent, alone or in combination with the Miura patent, fails to teach or suggest the elements of the claims. See M.P.E.P. § 2143 (stating that in order to establish a *prima facie* case of obviousness for a claim, the prior art references must teach or suggest all the claim limitations).

In particular, the Miura patent does not cure the deficiencies of the Arimilli patent discussed at length above with respect to Claims 1 and 14. Therefore, for reasons similar to those discussed above, Applicants respectfully submit that amended Claims 1 and 14 are not obvious in view of the Arimilli and Miura patents.

Claims 3 and 16, which depend from Claims 1 and 14 respectively, are believed to be patentable for at least the same reasons articulated above with respect to Claims 1 and 14, and because of the additional features recited therein.

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CONCLUSION

In view of the foregoing amendments and remarks, Applicants respectfully submit that the pending claims are now in condition for allowance and request reconsideration of the rejections. If it is believed that a telephone conversation would expedite the prosecution of the present application, or clarify matters with regard to its allowance, the Examiner is invited to contact the undersigned attorney at the number listed below.

No fee is believed to be due. However, the Commissioner is hereby authorized to charge payment of any required fees associated with this Communication or credit any overpayment to Deposit Account No. 23-1209.

Respectfully submitted,

Date: March 23, 2006

By: _____
Jason T. Evans, Esq.
Reg. No. 57,862

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